DETAILED ACTION

1. Claims 1-6 and 8-18 have been considered. Claim 7 cancelled as per Applicant's request. Claims 1-3, 6, 8-10, and 13-18 amended as per Applicant's request.

2. Examiner notes the entry of the following papers:

- Amendment to the specification filed 1/13/2010
- Amendment to the claims and remarks filed 1/13/2010
- Replacement drawings filed 1/13/2010

Drawings

3. The drawings submit on 1/13/2010 are deemed acceptable for examination proceedings.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1-6 and 8-18 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. In Claim 1, it is claimed that the exiting signal

is sent during a pipeline period immediately before a last cycle of the command exiting the pipeline, and that as a result of that signal, a new command is inserted into the pipeline. However, Figure 5 clearly shows new command G being inserted during Stage 1, when the last cycle of the command exiting the pipeline is Stage 3 (making the one immediately before that 2). This conflicts with the drawings, and thus appears to lack written description. Examiner will interpret the claim as it is written, however, clarification is required in the next action.

6. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

7. Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Claim 4 indicates that the exiting signal is released two stages before the new command enters the pipeline, however, Claim 1 appears to indicate that the new command is inserted in response to the exiting signal, which is only one stage before the new command enters the pipeline. However, this may be due to the claim not being clear as to when the new command is actually inserted in response to the exiting signal, or the Examiner not fully understanding the claim language, but either way, the claim appears to be inconsistent with the drawings and Claim 1. Clarification is required.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

9. Claims 1, 4-6, 8-10 and 15-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Hennessy et al. ("Computer Organization and Design, herein Hennessy).

10. Regarding Claim 1, Hennessy teaches: An overlapping command submitting method of dynamic cycle pipeline, for a chip having a pipeline including a plurality of stages, comprising the following steps:

(a) reading the command from a command buffer and storing it in a command register (Page 499: reading from the instruction memory and storing in the IF/ID pipeline register);

(b) decoding the command (Page 499; Page 450 Decode stage);

(c) preprocessing operators of the command (Page 469 Fig. 6.29), preparing initial operators of each stage of the pipeline, and storing them into an initialization register (Page 499 storing in ID/EX pipeline register);

(d) judging whether the pipeline is not full, if it is not full, directly inserting a new command (489-491 absent a stall, new instruction is automatically inserted), otherwise, waiting for an exiting signal from the command in the pipeline, the exiting signal being sent during a pipeline period immediately before a last cycle of the command exiting the

pipeline (Page 492, Figure 6.46, the forwarding unit's control signals to the ALU mux inputs, which are available as soon as it finishes the ALU stage, in the memory stage, which is one stage before the last cycle it is in the pipeline),

(e) after receiving the exiting signal, judging whether there is command relevance between the new command to be inserted and an old command to exit, if yes, then inserting the new command after the old command exit (Pages 476-477, if instruction B depends upon instruction A, it must be inserted after instruction A exits); otherwise, performing a next step (if there is no dependency, then there is no need to stall and wait);

(f) when the old command is in the last cycle of the pipeline, submitting the new command to the pipeline (Page 481, Figure 6.37, a command can be entered into the pipeline as soon as the command upon which it depends has it's result (in its last cycle));

wherein the new command and the old command each contain a field (Page 477, an operand),

wherein step (e) includes determining whether there is any field conflict between the new command and the old command (Page 478, detecting the hazard),

wherein if there is any field conflict between the new command and the old command, then a field branch is created (Page 492, the multiplexer connected to the ALU), the field branch including a major current register for storing the field of the new command (Page 492, the major current register corresponds to the value read from the register file) and a branch current register for storing the field of the old command (Page

480, the pipeline register holding the forwarded data), the field of the new command being added into the pipeline when submitting (Page 481, see the timing chart, the value is read from the register file when it leaves the register file stage), and the field of the old command being entered into the branch current register and maintained in the field branch until the old command uses the field for the last time (Page 480),

wherein the major current register and the branch current register are connected to a hardware processing module through a multi-route switch (Page 492, the multiplexer is the switch),

wherein if the new command is processed by the hardware processing module, the hardware processing module receives an input of the major current register in which the field of the new command is stored, and if the old command is processed by the hardware processing module, the hardware processing module receives an input from the branch current register in which the field of the old command is stored (Page 492 and 481, the forwarding logic selects either the old value or the new value, depending on which is appropriate, and sends that value to the processing module (the ALU)), and

wherein if there is no field conflict, a field switch is conducted in a corresponding pipeline segment after submitting (Page 466, the value is read from the register file if there is no required forwarding).

11. Regarding Claim 4, Hennessy teaches: The command submitting method of Claim 1, wherein the exiting signal is released two stages before the new command

enters the pipeline stage (Page 492, the forwarding from memory to the ALU stage a 2-stage difference).

12. Regarding Claim 5, Hennessy teaches: The command submitting method of Claim 1, wherein the command relevance means that the new command and the old command cannot share the hardware processing module in the same pipeline stage (Pages 476-477).

13. Regarding Claim 6, Hennessy teaches: The command submitting method of Claim 1, wherein in the Step (e), it is also judged in which stage of the pipeline field switch shall be conducted for the new command and the old command, and the field switch is completed in the corresponding pipeline stage where the new command and old command overlaps (Pages 476-479 and 492, the forwarding logic has to choose the appropriate feedback path).

14. Regarding Claim 8, Hennessy teaches: The command submitting method of Claim 1, characterized wherein in the Step (c), it is required to provide an initial status of each command when each command enters the pipeline (Page 469 Fig. 6.29 -- every instruction has its initial status provided).

15. Regarding Claim 9, Hennessy teaches: The command submitting method of Claim 1, wherein each command includes reading/writing memory commands (MIPs

data transfer instructions), reading/writing control register commands (MIPs move instructions) and various searching commands (MIPs Arithmetic Instructions that search for operands; moreover, all instructions can be used as part of searching algorithms).

16. Regarding Claim 10, Hennessy teaches: A chip on which the method according to Claim 1, is carried out having the dynamic cycle pipeline, comprising: interface of host computer (Page 499), input buffer (IF/ID pipeline register), command processing unit (Control), and result unit (Write Back Stage); the command processing unit comprises: command interpreter (Multiplexers receiving control signals & ALU control) and pipeline performing unit (anything in 499); characterized in that the command interpreter further comprises: command buffer controller (pipeline registers), command register (portion of IF/ID pipeline register holding opcodes), operator processing unit (ALU control), pipeline initialization register and control automaton (EX/ME pipeline register/ALU control), which are connected in order; the control automaton controls the command buffer controller to read a command from the command buffer (ALU control completes this), and stores the command into the command register; the control automaton decodes the command (Decode stage), and controls the operator processing unit to prepare initial operators of each pipeline stage according to a type of the command, and stores them into the pipeline initialization register (499).

17. Claims 15-18 are substantially similar to Claim 10, and are rejected for the same reasons set forth in the Claim 10 rejection above.

Claim Rejections - 35 USC § 103

18. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

19. Claims 2, 3, and 11-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hennessy, further in view of Vaglica (U.S. Patent No. 5,084,814).

20. Regarding Claim 2, Hennessy teaches: The method of Claim 1, but fails to teach: wherein the Step (b) also includes a step of judging whether there is an illegal command, if there is, then deleting the illegal command and returning to Step (a), otherwise, conducting the next step.

Vaglica discloses an illegal instruction detector and going to the next instruction if such a detection is made (Column 9, Lines 48-68).

Hennessy is silent towards any detection of illegal commands, and deleting them. However, Vaglica discloses a breakpoint system in which there is an illegal instruction detector, which allows the system to ignore the illegal instruction, and to instead execute the next instruction (Column 9, Lines 63-68). Vaglica further discloses that this detector provides several advantages, such as better data support features without requiring significant size for a debugging unit (Column 1, Lines 50-65). Given this

advantage, one of ordinary skill in the art would have been motivated to implement a system which can detect illegal instructions, and perform a variety of steps as a result of it, including deleting and ignoring it.

21. Regarding Claim 3, Vaglica teaches: The command submitting method of Claim 2, wherein said illegal command includes: a command with an incorrect command code and/or carrying unreasonable command parameters (Column 9, Lines 48-68).

22. Regarding Claim 11, Hennessy teaches: The command submitting method of Claim 2, wherein the exiting signal is released two stages before the new command enters the pipeline (Page 492, the forwarding from memory to the ALU stage a 2-stage difference).

23. Regarding Claim 12, Hennessy teaches: The command submitting method of Claim 2, wherein the command relevance means that the new command and the old command cannot share the hardware processing module in the same pipeline stage (Pages 476-477).

24. Claims 13 and 14 are substantially similar to Claim 10 (but depending upon Claims 2 and 3 respectively), and are taught by Hennessy for the reasons disclosed in the Claim 10 rejection above.

Response to Arguments

25. Examiner would like to express his appreciation for the interview conducted with the Applicant's representatives on 4/23/2010. The interview helped clarify the inventive concept, and has helped the Examiner conduct a more thorough search of the invention.

26. Examiner notes that due to the amendments to the claims, the objections and 112 rejections of the claims have now been overcome. Additionally, the drawing objections have been overcome as well.

27. In response to Applicant's arguments regarding that the claim amendments have overcome Hennessy, Examiner disagrees after a further consideration of the claims and the references. While the Examiner notes that the inventive concept is quite clearly distinct from Hennessy, and may in fact be allowable, as Examiner has not found any similar art to what the Applicant has explained to the Examiner to be the invention, at this point, Examiner does not believe it is fully expressed in the claims in such a way to overcome the rejection. From the Examiners understanding of the inventive concept, as described by the Applicant in the interview, during the first few cycles of a pipeline, before it is full, a second command can be inserted into the same pipeline stage as a first command, and be held in an idle state, until the first command is finished using the pipeline, and at that time, the second command "awakens", and takes over the spot of the first command, and then first command essentially becomes idle at that point.

Examiner notes that he may have this backward however, as the claims seem to indicate that if the pipeline is not full, then the command is just inserted into an empty slot, and sending a second command into the same pipeline stage is only done for a full pipeline, and additionally when an exiting signal is sent.

However, the Examiner does not believe that this concept is represented in the claims currently. The claims indicate that a new command is inserted into the pipeline if it is not full, and then determining if there is a relevance in a field, and if so, using the two-register system claimed to output the appropriate information. However, there is no clear recitation of whether or not the new command is sent to the same pipeline stage as the old command, the only thing that appears to be claimed at this point is that there are two instructions in the pipeline, in any stage, and that a system exists to resolve any field conflicts, which Examiner believes the forwarding logic of Hennessy reads upon.

Additionally, Examiner notes some other issues with the claims in regard to the drawings, which Examiner has made a new 112 rejection of. Claim 1 indicates that the exiting signal is sent during the pipeline period immediately before a last cycle, however, using Figure 5 as a guide, Stage 4 is where instruction A exits (thus, Stage 3 is the last cycle of the command). However, instruction G appears to be inserted into the pipeline in Stage 1, therefore, this is contrary to what the drawing is showing, therefore, it is not clear if what is being claimed is what is enabled by the specification, and leads to further confusion as to the subject matter.

28. Examiner believes that if the above issues can be clarified, the Hennessy reference will be clearly overcome, and the case may very well be allowable, however, a further search would likely be necessary to determine allowability, to check the exact claim language against any prior art. If the Applicant has any questions about this action, or wishes to discuss any potential amendments with the Examiner to help determine if the case will be able to overcome Hennessy or not, the Applicant is welcome to contact the Examiner at the phone number below to arrange for an interview, and the Examiner will attempt to assist in any manner he can to advance the case towards allowability.

Conclusion

29. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert Fennema whose telephone number is (571)272-2748. The examiner can normally be reached on Monday-Thursday, 9:30-6:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/
Supervisory Patent Examiner, Art Unit 2183

Robert Fennema
Examiner
Art Unit 2183

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